REMARKS

Applicant respectfully requests reconsideration of the present application in view of the foregoing amendments and in view of the reasons that follow.

Claims 1, 12, 14, 16, 18, 20 and 21 are currently being amended. Claim 2 has been cancelled.

This amendment changes and deletes claims in this application. A detailed listing of all claims that are, or were, in the application, irrespective of whether the claim(s) remain under examination in the application, is presented, with an appropriate defined status identifier.

After amending the claims as set forth above, claims 1, 3-18 and 20-22 are now pending in this application.

Amendments to the Specification

The title was objected to for not being descriptive. In response, Applicant has amended the title so that it is clearly indicative of the invention to which the claims are directed. Accordingly, Applicant requests reconsideration and that the objection be withdrawn.

Claim Rejections under 35 U.S.C. § 102

Claim 18 was rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 6,658,564 ("Smith"). In response, without agreeing or acquiescing to the rejection, Applicant amends claim 18 to further define the invention. In addition, Applicant respectfully traverses the rejection for the reasons set forth below.

Applicant relies on M.P.E.P. § 2131, entitled "Anticipation – Application of 35 U.S.C. § 102(a), (b) and (e)" which states, "a claim is anticipated only if each and every element set forth in the claim is found, either expressly or inherently described, in a single prior art reference." Applicant respectfully submits that Smith does not describe each and every element of the claims.

Claim 18 is directed to a program generation method including the steps of analyzing a control flow in which the control flow of an application program is analyzed, given the control flow of the whole application, completion data, structural information of an electronic computer and a plurality of command sets of the electronic computer as inputs, the application program is divided into processing units, and a command sequence intermediate code combining commands controlled by reconfigurable hardware that executes the divided processing units within an electronic computer is generated, implementing a command sequence procedure in which a command sequence is generated by translating the command sequence intermediate code into a form that can be executed by the electronic computer and generating program data in which the operational content of a processing unit is translated into a form that can be executed by the electronic computer, wherein the application program is divided so that each processing unit can be stored in a program data memory that holds a program creating a logic circuit for each processing unit in said reconfigurable hardware when the control flow of the application program is analyzed and divided into processing units in said control flow analysis procedure.

Accordingly, in the claimed invention configuration data of an application divided into a size below the size of reconfigurable hardware in the system, the system is operated by "switching" (replacing) the configuration data upon execution. This sequence of the switching corresponds to the command sequence. Further, since the configuration of reconfigurable hardware is formed of configuration data memory comprised of plurality of banks and their selector, it is possible to preload configuration data predetermined next to execute during operation of a reconfigurable hardware. The "command sequence" includes such load sequence of configuration data taking account of such a re-configurable hardware. Further, as disclosed at page 4, line 24 to page 5, line 4 of the present application, when this switching is executed by CPU, overhead occurs. Thus, the command sequence is controlled by the control device 60 and the configuration data is read out and written by the interface device 40 to the program data memory from an external memory device 10.

In sum, the claimed invention divides an application program into processing units and creates a logical circuit for every processing unit in reconfigurable hardware to improve processing speed at low cost. The present invention provides a concrete means for dividing an application program into processing units, generating a connection between the divided

processing units as a sequence and a control device which executes the sequence. Accordingly, the claimed invention can implement an application program that exceeds the capacity of the hardware present in the system.

Smith discloses a reconfigurable computer system. Smith discloses partitioning an application into blocks. *See* Col. 2, lines 4-8. Smith discloses that a partitioner automatically partitions a specification written in the system design language into software and hardware functions. *See* Col. 2, lines 24-26. However, Smith fails to disclose that the control flow of the whole application, completion data, structural information of an electronic computer and a plurality of command sets of the electronic computer are given as inputs in order to divide the application into processing units as claimed in independent claim 18. In contrast, Smith discloses using a specification algorithm, a set of constraints and a resource library as inputs. *See* Col. 10, lines 51-53. In addition, Smith discloses that its command sequence controls are executed by a virtual logic manager, which is a simple switching operation (col. 3, lines 1-4; col. 6, lines 53-56; col. 6, line 66 to col. 7, line 4). Thus, Smith does not disclose the preload operation and the generating method of the control sequence as claimed in claim 18.

Further, the examiner misunderstands the meaning of "command sequence implementation procedure" as a "compile method of software/hardware". In the claimed invention a command sequence implementation procedure is the instruction sequence that commands a timing to load configuration data of reconfigurable hardware or a timing for making the configuration data valid. This feature of the present invention is also different from interface function 86 (i.e., a method for transmitting (exchanging) processing data between SW and programmable logic of Smith. Accordingly, Applicant respectfully requests that the rejection be withdrawn and claim 18 be allowed.

Claim Rejections under 35 U.S.C. § 103

Claims 1, 12, 14 and 20 were rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,326,806 ("Fallside") in view of Smith. Claims 2-5, 16, 17, 21 and 22 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Fallside and Smith and further in view of U.S. Patent No. 6,034,538 ("Abramovici") and U.S. Patent No. 6,573,748 ("Trimberger"). Claims 6-7 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Fallside and Smith in further view of U.S. Patent No. 5,887,189 ("Birns et al."). Claims

8-9 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Fallside, Smith and Birns in further view of U.S. Patent No. 5,473,763 ("Stewart"). Claims 10 and 11 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Fallside and Smith in view of U.S. Patent No. 4,860,192 ("Sachs"). Claims 13 and 15 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Fallside and Smith in further view of Abramovici.

Applicant relies on M.P.E.P. § 2143, which states that to establish a prima facie case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation in the prior art to modify the reference. Second, there must be a reasonable expectation of success. Third, the prior art must teach or suggest all the claim limitations.

Claims 1 and 12 are directed to an electronic computer implemented using reconfigurable hardware. Claims 14 and 16 are directed to a control method for an electronic computer implemented using reconfigurable hardware. Claims 20 and 21 are directed to a computer program product which when executed performs a method implemented using reconfigurable hardware. Specifically, the above claims require a method and a processing device including having a program, wherein said program is generated, given a control flow of the application program, completion data, structural information of the electronic computer and a plurality of command sets of the electronic computer as inputs, by executing a control flow analysis procedure for generating a command sequence executed after each process, executing a command sequence implementation procedure for translating said command sequence into a data string, and executing a program data generation procedure for generating program data.

In sum, the claimed invention divides an application program into processing units and creates a logical circuit for every processing unit in reconfigurable hardware to improve processing speed at low cost. The present invention provides a concrete means for dividing an application program into processing units, generating a connection between the divided processing units as a sequence and a control device which executes the sequence. Accordingly, the claimed invention can implement an application program that exceeds the capacity of the hardware present in the system.

Fallside and Smith do not disclose, teach or suggest each and every element of independent claims 1, 12, 14, 16, 18, 20 and 21. Fallside is directed to a FPGA-Based

system. While Fallside teaches a control circuit for reconfiguring a FPGA in response to a predetermined condition, Fallside does not disclose, teach or suggest a method and a processing device having a program wherein said program is generated, given a control flow of the application program, completion data, structural information of the electronic computer and a plurality of command sets of the electronic computer as inputs, by executing a control flow analysis procedure for generating a command sequence executed after each process, executing a command sequence implementation procedure for translating said command sequence into a data string, and executing a program data generation procedure for generating program data. Similarly, while Smith mentions that functions of an application are partitioned into blocks, Smith fails to disclose that the control flow of the whole application, completion data, structural information of an electronic computer and a plurality of command sets of the electronic computer are given as inputs in order to divide the application into processing units as claimed in independent claims 1, 12, 14, 16, 18, 20 and 21. In contrast, Smith discloses using a specification algorithm, a set of constraints and a resource library as inputs. *See* Col. 10, lines 51-53.

Accordingly, Applicant respectfully request that the rejection be withdrawn and independent claims 1, 12, 14, 16, 18, 20 and 21 be allowed. Further, claims 3-11, 13, 15, 17 and 22 depend from one of independent claims 1, 12, 14, 16, 20 and 21 and should therefore be allowable for the reasons set forth above without regard to further patentable limitations cited therein.

For example, concerning claims 5, 17 and 22, the Office Action alleges that "FPGA_PROG" of Fallside is the same as "cancel_prg" of the present invention. However, FPGA_PROG executes initialization and does operate analogous to the cancel_prg as claimed in claims 5, 17 and 22. In addition, FPGA_INIT of Fallside is a signal for stopping a configuration and is different in operation from that of "halt" (halting processing) of the claimed invention. Concerning claims 6, Fallside does not disclose a read, interpret and execute the command. Further, CFG_MODE is setting of configuration method (Fig. 4), that is different from that of the command of the claimed invention. Accordingly, for these additional reasons Applicant requests that claims 3-11, 13, 15, 17 and 22 be allowed.

Conclusion

Applicant believes that the present application is now in condition for allowance. Favorable reconsideration of the application as amended is respectfully requested.

The Examiner is invited to contact the undersigned by telephone if it is felt that a telephone interview would advance the prosecution of the present application.

The Commissioner is hereby authorized to charge any additional fees which may be required regarding this application under 37 C.F.R. §§ 1.16-1.17, or credit any overpayment, to Deposit Account No. 19-0741. Should no proper payment be enclosed herewith, as by a check or credit card payment form being in the wrong amount, unsigned, post-dated, otherwise improper or informal or even entirely missing, the Commissioner is authorized to charge the unpaid amount to Deposit Account No. 19-0741. If any extensions of time are needed for timely acceptance of papers submitted herewith, Applicant hereby petitions for such extension under 37 C.F.R. §1.136 and authorizes payment of any such extensions fees to Deposit Account No. 19-0741.

Respectfully submitted,

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